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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,117	12/15/2003	Daniel Yellin	MP1493 151668	4852

65589 7590 02/08/2007
SCHWABE, WILLIAMSON & WYATT, P.C.
PACWEST CENTER, SUITE 1900
1211 S.W. FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No. 10/734,117	Applicant(s) YELLIN ET AL.	
	Examiner Freshteh N. Aghdam	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-31* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 29-31 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the first communication device is not coupled to any other elements in the communication system as described in claim 29.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-9 are rejected as being under 35 U.S.C. 101 because: the claimed invention is directed to a non-statutory subject matter because as a whole it does not accomplish a practical application. In order to accomplish a practical application, it must produce a: useful, concrete and tangible result." (Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility, pages 21-22) In other words, the tangible requirement does require that the claim must recite more than a 101 judicial exception. It is for the discovery or invention of some practical method or means of

producing a beneficial result or effect, that a patent is granted see Corning, 56 U.S. (15 How.) at 268, 14 L.Ed. 683. Claim 1 recites a method, however, there is no tangible result disclosed for this method. Claims 2-9 are dependent on the independent claim 1; therefore, they are also rejected under 35 U.S.C. 101.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilcocq et al (US 2004/0041638).

As to claim 1, Vilcocq discloses a method comprising building a linear model of an analog fractional-N phase locked loop unit including a bilinear model of loop filter of the phase locked loop, wherein the analog fractional-N phase locked loop includes a voltage controlled oscillator (Fig. 2, means 11-14; Par. 33-37 and 40-45); and determining a transfer function of a filter that is optimized according to predefined optimization criteria (Par. 12-13), wherein the optimization criteria relate to an input to said filter and an output to the voltage controlled oscillator (Fig. 2; Par. 12-13 and 40-45). Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would recognize that optimization criteria of Vilcocq not only includes the input of the voltage-

controlled oscillator (i.e. output of the loop filter) but also takes into the account the effects of the voltage-controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter to the linearized response of the phase locked loop variations.

As to claim 2, Vilcocq discloses that said model includes impairments of one or more components of the phase locked loop (Par. 38-39).

As to claim 3, Vilcocq discloses that the model includes phase noise (Par. 12-13).

As to claim 4, Vilcocq discloses that the model includes variations of parameters of phase locked loop unit from nominal values (Par. 38-39).

As to claim 5, Vilcocq discloses that determining the transfer function includes determining the transfer function to be optimized according to the predefined optimization criteria that includes a mean squared error of an input to the filter and an output to the voltage controlled oscillator (Par. 12-13).

As to claim 6, Vilcocq discloses determining the transfer function of the filter that is optimized based on performance characteristics (i.e. quality parameter(s)) estimation of the output of the voltage-controlled oscillator (Par. 12-13). Vilcocq is not explicit about determining the transfer function includes determining the transfer function to be optimized according to the predefined optimization criteria that includes spectral cleanliness of an output of the voltage controlled oscillator. However, one of ordinary skill in the art would recognize that spectral cleanliness of the voltage-controlled

oscillator is a quality parameter. Therefore, it would have been obvious to one of ordinary skill in the art to optimize the transfer function of the filter based on spectral cleanliness of the voltage-controlled oscillator in order to enhance performance of the digital modulation of a PLL synthesizer.

As to claim 7, Vilcocq inherently discloses selecting topology for the transfer function (Fig. 2, means 18, A(z)).

Claims 8-9, 14-22, 24, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilcocq et al, and further in view of Perrott et al (US 6,008,703).

As to claims 8-9, Vilcocq discloses all the subject matter claimed in claim 1, except for the digital filter is a finite impulse response (FIR) or an infinite impulse response (IIR) filter. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

As to claim 14, Vilcocq discloses a fractional-N sigma-delta modulator comprising: a digital filter with a transfer function, the filter is coupled to an input of a sigma-delta converter (Fig. 2, means 15 and 18); and a fractional-N phase locked loop

unit coupled to an output of the sigma-delta converter (means 11-14). Vilcocq is not explicit about the transfer function of the digital filter is a finite impulse response transfer function. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

As to claim 15, Vilcocq discloses that the transfer function is substantially equivalent to a transfer function of a minimum mean squared error equalizer (Par. 12-13).

As to claim 16, Vilcocq discloses that the digital values of the filter are to adjusted so that said transfer function is optimized according to predefined optimization criteria (Par. 12-13 and 40-45).

As to claim 17, Vilcocq discloses that the optimization criteria includes a mean squared error of an input to the filter and an output to a voltage controlled oscillator of the fractional-N phase locked loop unit (Fig. 2; Par. 12-13 and 40-45). Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would recognize that optimization criteria of Vilcocq not only includes the input of the voltage-controlled

oscillator (i.e. output of the loop filter) but also takes into the account the effects of the voltage-controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter to the linearized response of the phase locked loop variations.

As to claim 18, Vilcocq discloses determining the transfer function of the filter that is optimized based on performance characteristics (i.e. quality parameter(s)) estimation of the output of the voltage-controlled oscillator (Par. 12-13). Vilcocq is not explicit about determining the transfer function includes determining the transfer function to be optimized according to the predefined optimization criteria that includes spectral cleanliness of an output of the voltage controlled oscillator. However, one of ordinary skill in the art would recognize that spectral cleanliness of the voltage-controlled oscillator is a quality parameter. Therefore, it would have been obvious to one of ordinary skill in the art to optimize the transfer function of the filter based on spectral cleanliness of the voltage-controlled oscillator in order to enhance performance of the digital modulation of a PLL synthesizer.

As to claim 19, Vilcocq discloses a fractional-N sigma-delta modulator comprising: a sigma-delta modulator (Fig. 2, means 15); a fractional-N phase locked loop unit coupled to an output of said sigma-delta modulator and including a voltage controlled oscillator (means 11-14); and a digital filter with a transfer function, the filter coupled to an input of the sigma-delta modulator, wherein the transfer function is not an inverse of a transfer from an output of the filter to an output of the voltage-controlled

oscillator (Par. 8-13). Vilcocq is not explicit about the transfer function of the filter is an infinite impulse response. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

As to claim 20, Vilcocq discloses that the digital values of the filter are to be adjusted so that the transfer function is optimized according to predefined optimization criteria (Par. 8-13).

As to claim 21, Vilcocq discloses that the optimization criteria are related to an input to the filter and an output to a voltage controlled oscillator of the fractional-N phase locked loop unit (Fig. 2; Par. 12-13 and 40-45). Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would recognize that optimization criteria of Vilcocq not only includes the input of the voltage-controlled oscillator (i.e. output of the loop filter) but also takes into the account the effects of the voltage-controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter to the linearized response of the phase locked loop variations. Also, Perrott

discloses that filter does not require performing the precise inverse of the phase locked loop in order to reduce and/ or simplify hardware complexity (Col. 10, Lines 6-21; Col. 11, Lines 1-14). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reason stated above.

As to claim 22, Vilcocq discloses all the subject matter claimed in claim 20, except for the optimization criteria includes spectral cleanliness of output of the voltage controlled oscillator. However, one of ordinary skill in the art would recognize that spectral cleanliness of the voltage-controlled oscillator is a quality parameter. Therefore, it would have been obvious to one of ordinary skill in the art to optimize the transfer function of the filter based on spectral cleanliness of the voltage-controlled oscillator in order to enhance performance of the digital modulation of a PLL synthesizer.

As to claim 24, Vilcocq discloses all the subject matter claimed in claim 23, except for the transfer function of the adaptive filter is a finite impulse response. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

As to claims 30-31, Vilcocq discloses all the subject matter claimed in claim 29, except for the digital filter is a finite impulse response (FIR) or an infinite impulse response (IIR) filter. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vilcocq et al, and further in view of Hasson (US 2003/0123566).

As to claim 26, Vilcocq discloses a communication device comprising at least an antenna; a power amplifier coupled to the antenna; and a fractional-N sigma-delta modulator coupled to the power amplifier (Par. 1), the modulator including at least a filter coupled to an input of a sigma-delta converter (Fig. 2, means 15 and 18); and a fractional-N phase locked loop unit coupled to an output of the sigma-delta converter (means 11-14), wherein a transfer function of said filter is to be optimized according to predefined optimization criteria (Par. 8-13). Vilcocq is not explicit about the antenna being a dipole antenna. Hasson discloses a communication device comprising a diploe

antenna (Fig. 1, means 108; Claim 6); a power amplifier coupled to the antenna (means 106); and a sigma-delta modulator coupled to the power amplifier (means 102). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Hasson with Vilcocq in order to transmit the modulated signal via a dipole antenna since dipole antennas show high antenna efficiency and integration flexibility.

Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilcocq et al and Hasson, further in view of Perrott et al.

As to claims 27-28, Vilcocq and Hasson disclose all the subject matter claimed in claim 26, except for the digital filter is a finite impulse response (FIR) or an infinite impulse response (IIR) filter. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq and Hasson for the reasons stated above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10-13, 23, 25, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Vilcocq et al.

As to claim 10, Vilcocq discloses a method comprising adjusting digital values of a filter to compensate for variations in an analog fractional-N phase locked loop (Par. 7-13; Fig. 2, means 18).

As to claim 11, Vilcocq discloses adjusting the digital values includes adjusting the digital values to compensate at least for variations in voltage, temperature, aging, or any combination thereof (Par. 38-39).

As to claim 12, Vilcocq discloses adjusting the digital values includes adjusting the digital values to compensate at least for variations of parameters of the phase locked loop unit from nominal values (Par. 38-39).

As to claim 13, Vilcocq discloses determining adjusted digital values so that a transfer function of the filter is optimized according to predefined optimization criteria (Par. 12-13).

As to claim 23, Vilcocq discloses a fractional-N sigma-delta modulator comprising: an adptive filter coupled to an input of a sigma-delta modulator (Fig. 2, means 15); and a franctional-N phase locked loop unit coupled to an output of said sigma-delta modulator (means 11-14).

As to claim 25, Vilcocq discloses that the fractional-N phase locked loop unit includes a voltage-controlled oscillator, and wherein a transfer function of said adaptive filter is not an inverse of a transfer function from an output of the filter to an input of the voltage controlled oscillator (Fig. 2; Par. 8-13).

As to claim 29, Vilcocq discloses a communication system comprising a receiver and a transmitter (Par. 1), wherein the transmitter including at least a fractional-N sigma-delta modulator (Fig. 2, means 15); a filter coupled to an input of a sigma-delta modulator (means 18); and a fractional-N phase locked loop unit coupled to an output of the sigma-delta converter (means 11-14), wherein a transfer function of the filter is to be optimized according to predefined optimization criteria (Par. 8-13).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Eriksson et al (US 6,047,029) see figures 5-6; and Liu (us 2005/0058219) see paragraphs 25, 31, and 54.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is (571)

272-6037. The examiner can normally be reached on Monday through Friday 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Freshteh Aghdam
Examiner
Art Unit 2611

F.A

KEVIN BURD
PRIMARY EXAMINER